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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/676,311	09/30/2000	Nhon Toai Quach	42390P5727	4002

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EXAMINER	
LOHN, JOSHUA A	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/676,311	QUACH ET AL.	
	Examiner	Art Unit	
	Joshua A Lohn	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-8,11-13 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,11-13 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 8/24/2004 have been fully considered but they are not persuasive. In response to applicants arguments that an exception, such as the General Protection Fault of the Pentium Pro Family Developer's Manual, Volume 2, will not be triggered by corrupted memory, the examiner respectfully disagrees. The General Protection Fault is a fault that occurs on any memory reference and otherwise cannot be handled, this would inherently include faults generated by the attempts to access corrupted memory. Applicant states that Ross prefers to handle the exceptions that a calling program can deal with (Ross, col. 1, line 58, through col. 3, line 25), however Ross provides a mechanism to delay fault reporting in a speculative load where the calling program and the operating system cannot resolve the exception generating fault (Ross, col. 10, lines 29-65). The desire of Ross to include handling of exceptions that are not able to be repaired (Ross, col. 10, lines 60-65) or not explicitly described in the disclosure (Ross, col. 10, lines 43-44), would provide significant motivation to handle such exception as the General Protection Fault of the Pentium Pro Family Developers Manual, Volume 2, that may be raised in speculative memory operations. This is indicated in the new grounds of rejection set forth below with respect to claims 1-3, 6-8, 11-13, and 16-18.

Claim Rejections - 35 USC § 103

Claims 1-3, 6-8, 11-13, and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ross et al., United States Patent number 5,915,117, published June 22, 1999 in view of the Pentium® Pro Family Developer's Manual, Volume 2: Programmer's Reference Manual, published 1996.

As per claim 1, Ross discloses a method of handling memory errors, in the form of memory exceptions, see column 1, lines 13-16. Ross also discloses receiving and retaining control of a machine from an executing program after an error in a memory value is detected while executing a memory load request issued by the executing program to retrieve the memory value from the memory. This is shown in figure 1, where the memory handler controls the flow of instructions during the execution of a load operation initiated by the executing program, see boxes 102-110, where all load requests and any exceptions, or errors, are handled before the load execution is completed by the processor and control is returned to the executing program. All load requests include memory values, in the form of instructions, see column 7, lines 6-67. Ross discloses receiving a speculative load indication that is true if the memory load request was issued speculatively, the speculative load indicator being provided during compilation, see column 3, lines 49-51. Ross also discloses reading a fault deferral indication that is true if faults caused by errors in memory values can be deferred, the fault deferral indication being set before the error in the memory is detected, the fault deferral indication being the ITLB.ed entry, see column 6, lines 48-50, which is set during compilation and reflects faults caused by errors in the instruction values located in memory, and before any execution based error can occur, see column 9, lines 19-21. If the fault deferral indication is true and the speculative load indication

is true, Ross discloses providing an error indication that the returned memory value is invalid. This is disclosed in figure 1, where if fault deferral indication, 105, and speculative load indication, 104, are both true the hardware will return a deferred exception indicator in the destination register to indicate the memory value is invalid, 109. Finally, Ross discloses returning control of the machine to the executing program at the point after previous load execution, 111 in figure 1. Ross fails to explicitly disclose the fault deferral being able to handle an exception caused by an error such as a corruption of a memory value.

Pentium Pro Family Developers Manual discloses that a known exception type is a General Protection Fault, which is known to handle all general types of errors in a memory access, and would inherently include faults such as those generated by corrupted memory values (Pentium Pro Family Developer's Manual, page 4-11).

It would have been obvious to one skilled in the art at the time of the invention to include this General Protection Fault exception in the list of those able to be handled by the invention of Ross.

This would have been obvious because Ross discloses a desire to not be limited by the exceptions explicitly listed in the disclosure (Ross, col. 10, lines 40-44). Ross further discloses a desire to provide fault deferral mechanisms to handle an exception generated by a fault that may not be able to be corrected, such as any corrupted memory values that would generate a General Protection Fault (Ross, col. 10, lines 61-65). Thus it would have been obvious to provide an exception resulting from corrupt memory in the invention of Ross to further improve the disclosed desire to defer a broad range of exceptions generated by speculative memory operations.

As per claim 2, Ross discloses the error indication is a flag bit associated with the returned memory value. This is shown in the PSR.ed value that indicates a deferred exception, see column 10, line 66 through column 11, line 25. This deferred exception relates directly to the load operation of the instruction from memory, see column 10, lines 51-67.

As per claim 3, Ross discloses the error indication is setting the returned memory value to an invalid value. This is shown in the return value to the destination register being the deferred exception indicator, which is inherently an invalid memory value to allow it to be an accurate indicator.

As per claims 6-8, the limitations of these claims are the same as those rejected for claims 1-3 above, but in the form of a machine-readable medium. Ross teaches of implementing the methods described above in software, which is a machine-readable medium, see column 1, lines 14-17.

As per claims 11-13, the limitations of these claims are the same as those rejected for claims 1-3 above, but include an interface to receive a value from a memory coupled to the machine. Ross discloses the use of memory loads, which require that an interface exist to receive these values from memory, see column 3, lines 30-35.

As per claims 16-18, the limitations of these claims are the same as those rejected for claims 1-3 above, but including a machine-readable medium executed by the machine. The ability to load from memory indicates that Ross discloses a coupling between memory and the machine executing the invention, see column 3, lines 30-35. Ross discloses this machine executing machine-readable software, see column 1, lines 14-17.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (703) 305-3188. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAL

SCOTT BADERMAN
PRIMARY EXAMINER